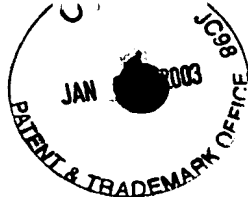


Docket No. 210067US2



#46
1506
H603

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Hidemasa ZAMA, et al.

SERIAL NO: 09/883,959

GAU: 2819

FILED: June 20, 2001

EXAMINER: TAN, V.

FOR: SEMICONDUCTOR INTEGRATED CIRCUIT, LOGIC OPERATION CIRCUIT, AND FLIP FLOP

REQUEST FOR EXTENSION OF TIME
UNDER 37 C.F.R. 1.136

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

It is hereby requested that a **two and three** month extension of times be granted to January 1, 2003 for

- ☐ filing a response to the Official Action dated:
- ☐ responding to the requirements in the Notice of Allowability dated:
- ☐ filing the Formal Drawings. The Issue Fee due has been timely filed.
- ☐ responding to the Notice to File Missing Parts of Application dated:
- ☒ filing a Notice of Appeal. A timely response to the final rejection, due October 1, 2002 has been filed.

filing an Appeal Brief. A Notice of Appeal was filed on:

- ☐ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee amount shown below is reduced by one-half.

The required fee of \$820.00 is enclosed herewith by check and any further charges may be made against the Attorney of Record's Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Gregory J. Maier

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22850

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(OSMMN 10/01)

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W. Todd Baker

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Eckhard H. Kuesters
Registration No. 28,870

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